

REMARKS

Reconsideration of this application as amended is respectfully requested.

In the final Office Action dated February 4, 2005, claims 1-24 were pending and rejected. A response was filed and an advisory action was issued. In the advisory action, the response was not entered. In this response, no claim has been canceled. Claims 1, 9, 17, and 20-24 have been amended. No new matter has been added.

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph. In view of the foregoing amendments, it is respectfully submitted that the rejection has been overcome.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,229,929 of Lynch et al. ("Lynch") in view of U.S. Patent No. 5,946,349 of Raghunath ("Raghunath"). In view of the foregoing amendment, it is respectfully submitted that claims 1-24 include limitations that are not disclosed or suggested by the cited references.

Specifically, independent claim 1 recites as follows:

1. A method comprising:
receiving a sequence of image data to compress; and
specifying scalar quantization with a power of two step size using three bit values to apply to the sequence of image data, wherein the three bit values specify a number of bitplanes to be truncated during the quantization, and wherein a value with all three bits having an identical logical value indicates that all bitplanes are to be truncated, each of the bitplanes corresponding to a one-bit-per-pixel image capable of being displayed overlaying with one or more other bitplanes.

(Emphasis added)

Independent claim 1 includes limitations that three-bit values (e.g., only using 3 bits) are used to specify the number of bitplanes to be truncated during the quantization, where a value with all three bits having a logical value of one indicates that all bitplanes are to be truncated, wherein each bitplane corresponds to a one-bit-per-pixel image and each of one-bit-per-pixel

images (e.g., bitplanes) can be displayed overlaying with each other. For example, three-bit values having from 0-6 indicate 0-6 bitplanes to be truncated respectively, while a value of 7 (e.g., all three bits have a logical value of 1) indicates that all bitplanes (which may be more than 6 bitplanes as recited in claims 21-24 as amended) to be truncated. It is respectfully submitted that the above limitations are absent from Lynch.

Although Lynch indicated that certain LSB bits of coefficients are to be truncated in a power of two step, it is unclear how Lynch specifies the number of bits to be truncated. Specifically, Lynch fails to disclose that the number of the bitplanes that may be translated into number of bits in power of two step is specified using a value only containing three bits, where a value having all bits as the same logical value indicates that all bitplanes are to be truncated. It is well known in the art that a bitplane corresponds to a one-bit-per-pixel image and several bitplanes can be displayed overlaying each other to form a whole image. It is respectfully submitted that Lynch fails to disclose that the power of two step is used to indicate the number of bitplanes to be truncated.

Similarly, Raghunath fails to disclose or suggest the above limitations. Raghunath is not related to image or video encoding processes. Rather, Raghunath is related to an adaptive equalizer system, where the general adaptation process for an adaptive filter or equalizer operates on the tap coefficients of such a filter or equalizer by iteratively adjusting such coefficients to process toward the achievement of a desired objective (e.g., SNR ratio) above a desired threshold (see, col. 2, lines 3 to 9 of Raghunath).

Specifically, Raghunath is trying to eliminate those “false” coefficients during the DSP processes. For example, Raghunath truncates any negative coefficient, where a negative coefficient near zero will occur as all “1”s in two’s-complement representation (e.g., at least the sign bit having a logical value of “1”). See, for example, col. 2, lines 45-61 and col. 5, lines 28-

43 of Raghunath. Thus, the truncation bits of Raghunath do not represent a number of bitplanes to be truncated as recited in claim 1.

In addition, there is no suggestion within Lynch and Raghunath to combine with each other because, as described above, they are related to significantly different areas. Even if they were combined, such a combination still lacks the limitations set forth above. Therefore, it is respectfully submitted that independent claim 1 is patentable over Lynch in view of Raghunath.

Similarly, independent claims 9, 17, and 20 include limitations similar to those recited in claim 1. Thus, for the reasons similar to those discussed above, independent claims 9, 17, and 20 are patentable over Lynch in view of Raghunath.

Given that the rest of the claims depend from one of the above independent claims, at least for the reasons similar to those discussed above, it is respectfully submitted that the rest of the claims are patentable over Lynch in view of Raghunath. Withdrawal of the rejections is respectfully requested.


In view of the foregoing, Applicants respectfully submit the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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Kevin G. Shao
Attorney for Applicant
Reg. No. 45,095
Kevin_shao@bstz.com

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300